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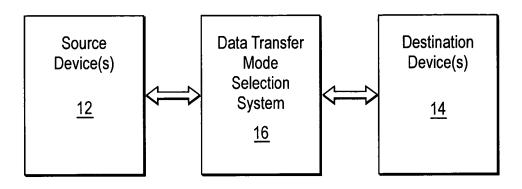


FIG. 1

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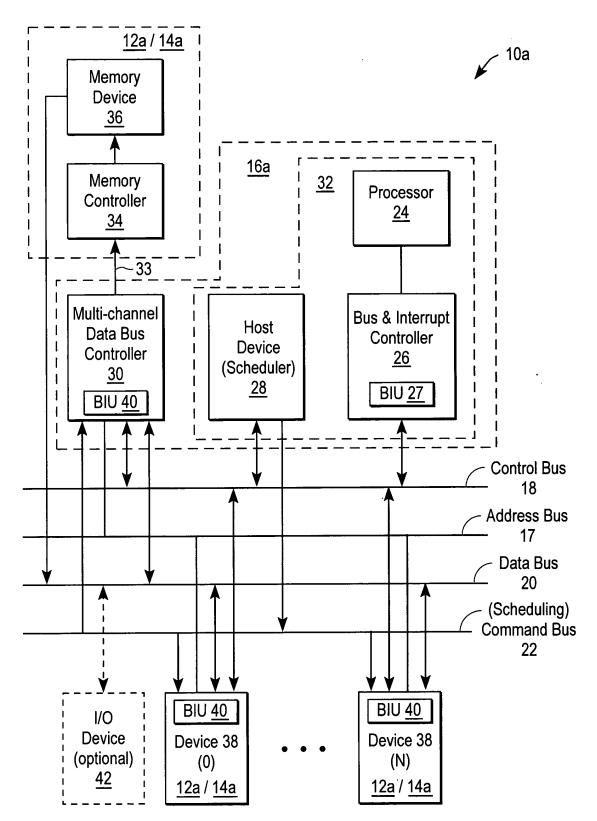


FIG. 2

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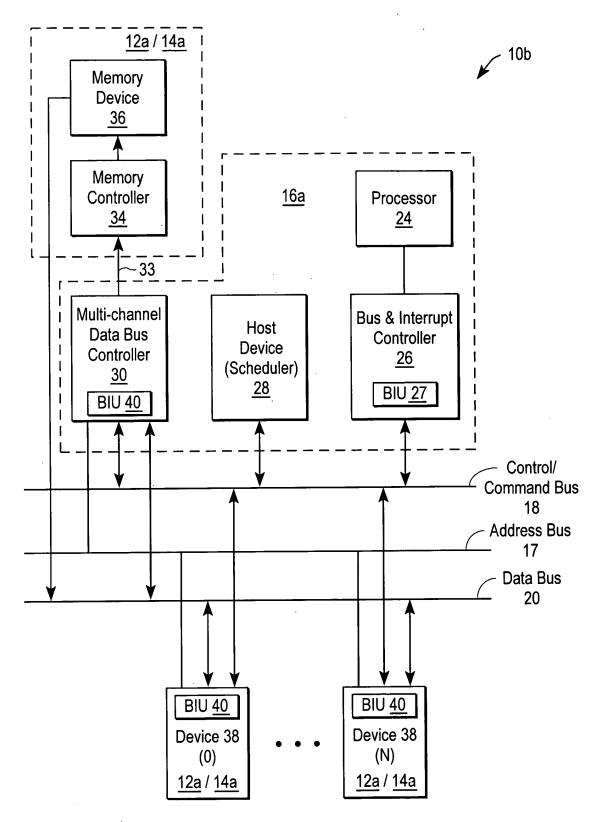


FIG. 3

Processing

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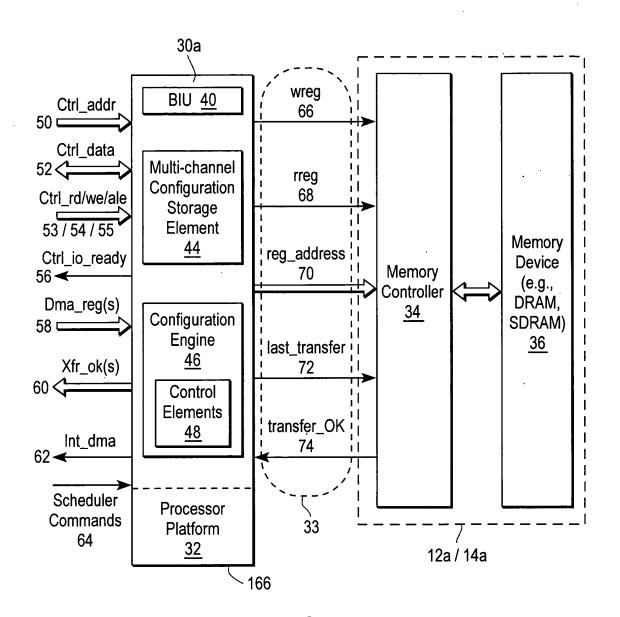


FIG. 4

86a

88a

Mode 6 bit

па́

where 0 < m < n

(e.g., n=31)

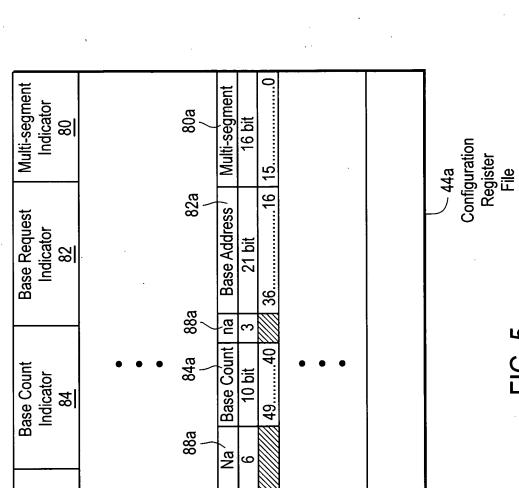
Indicator 86

Reserved 88

Ö

Mode

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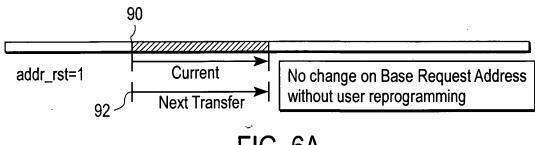


FIG. 6A

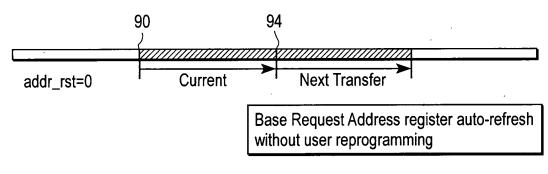


FIG. 6B

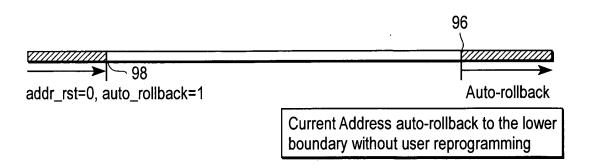


FIG. 6C

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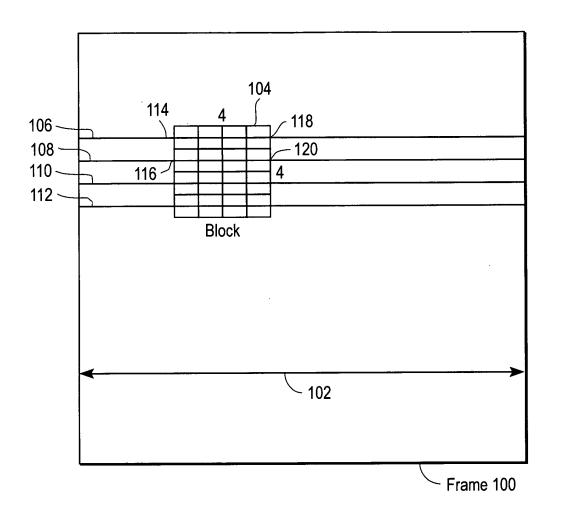


FIG. 7

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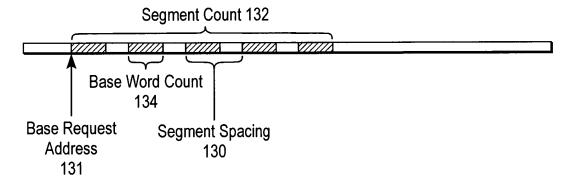


FIG. 8

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Signal Flow Diagram For Virtual Channel Mode

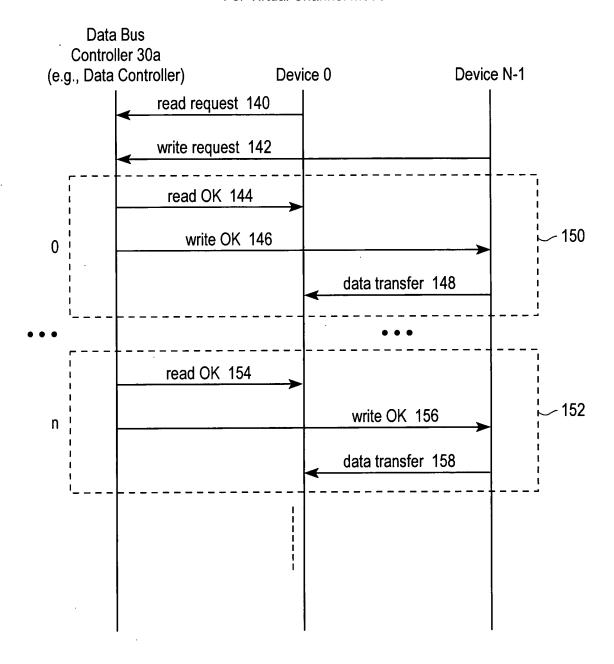
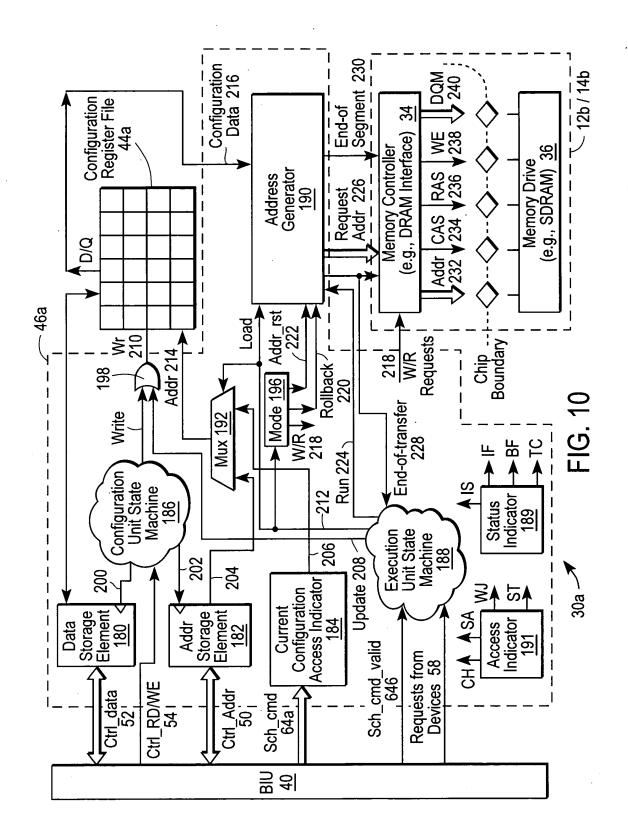


FIG. 9

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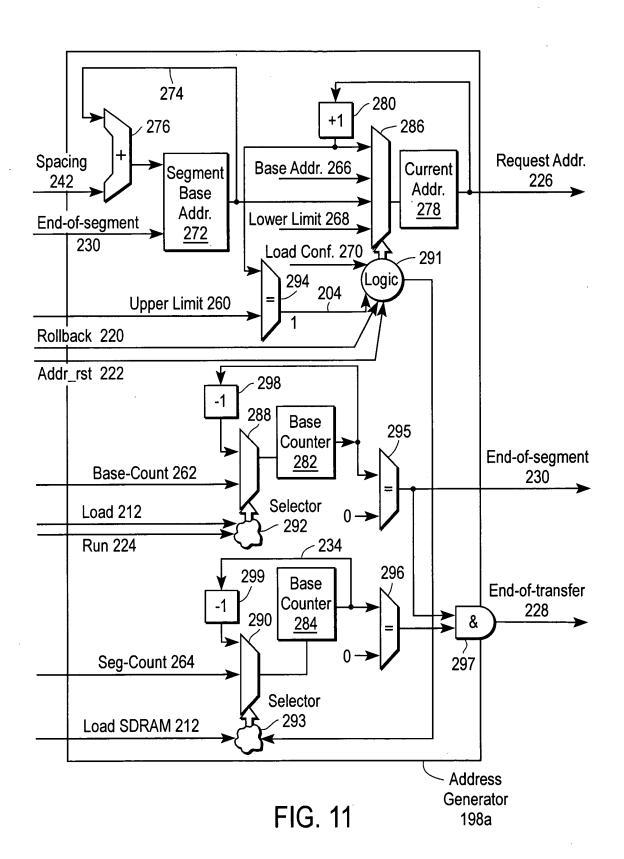


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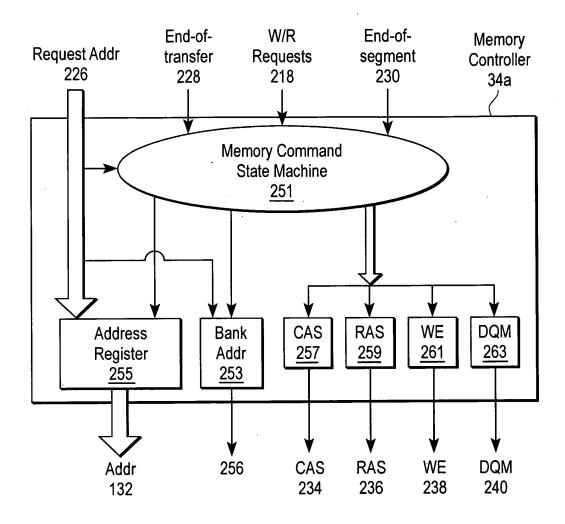
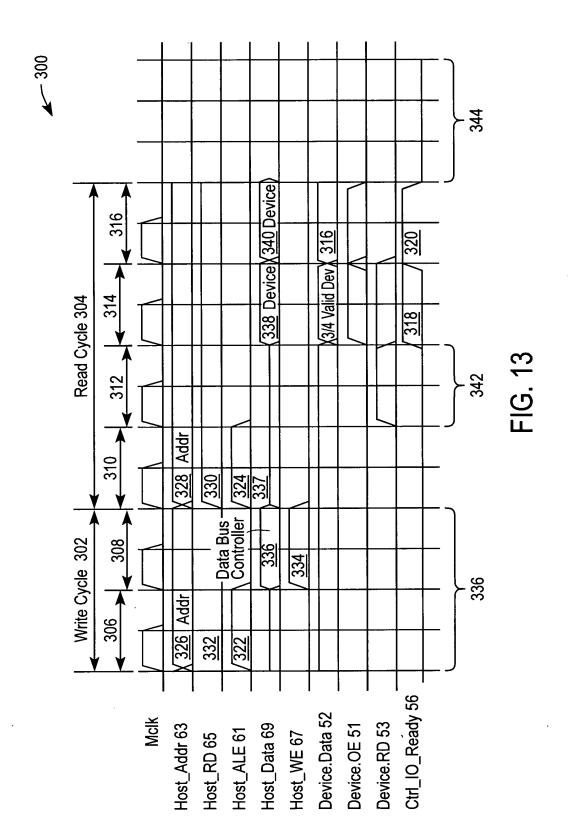
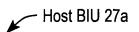


FIG. 12

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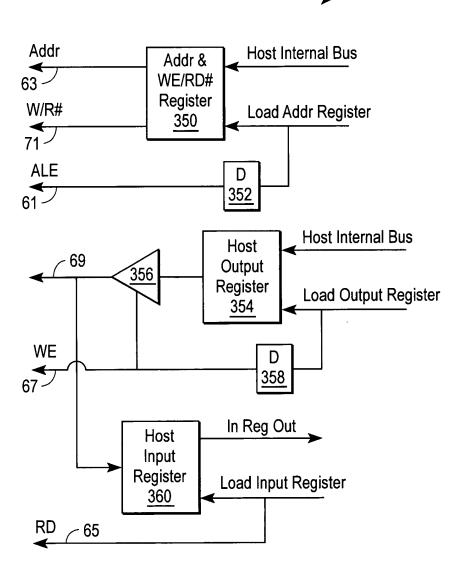


FIG. 14

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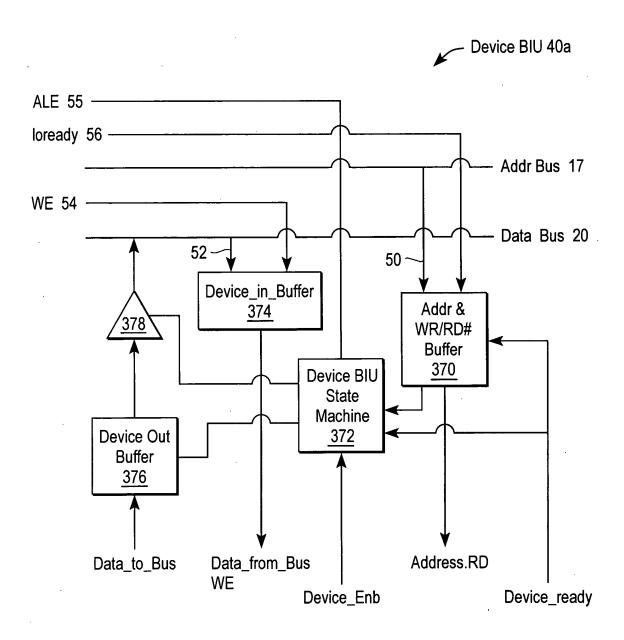
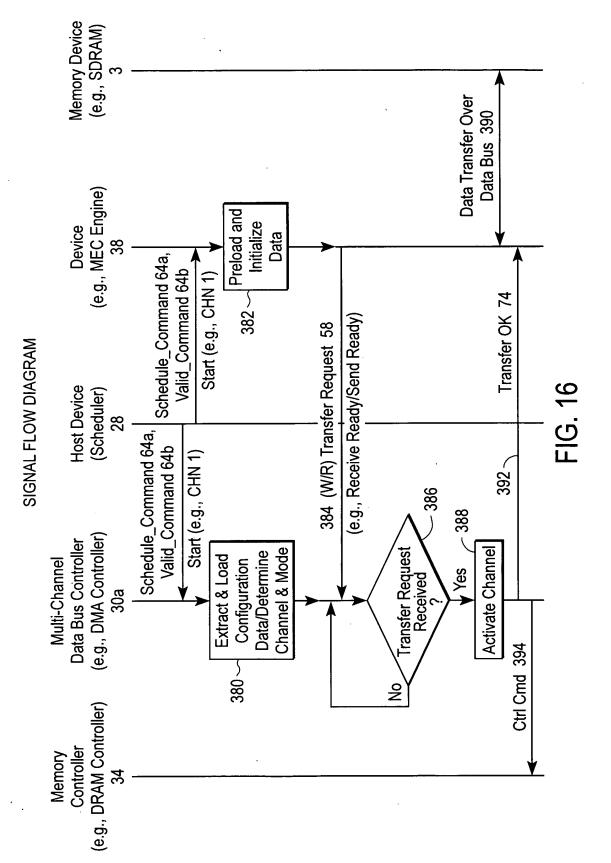


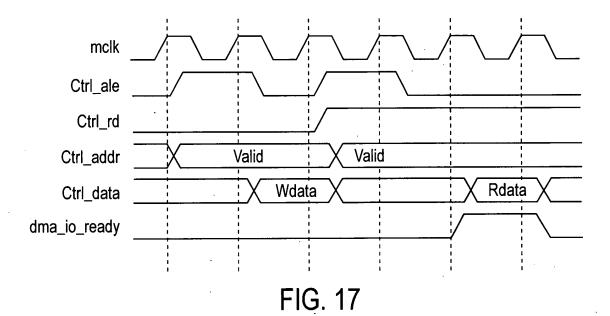
FIG. 15

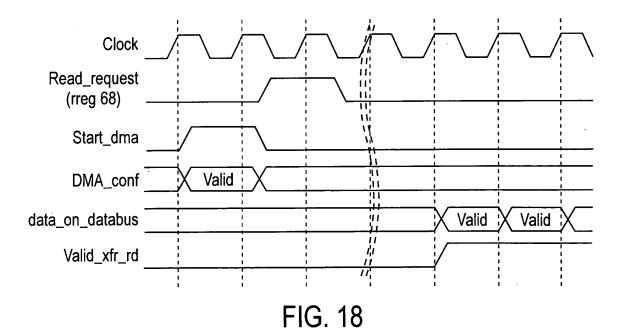
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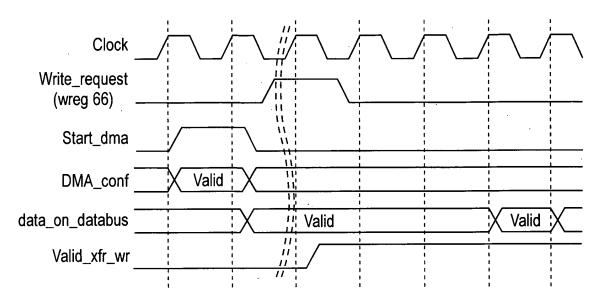


FIG. 19

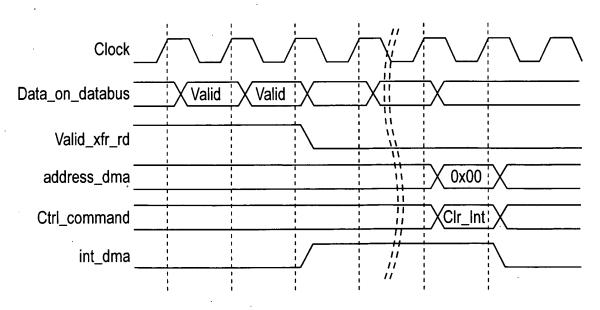


FIG. 20

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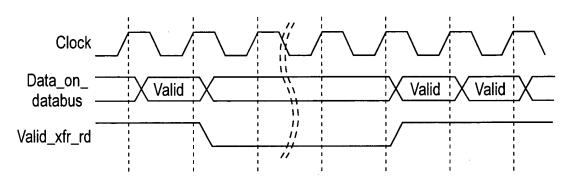


FIG. 21

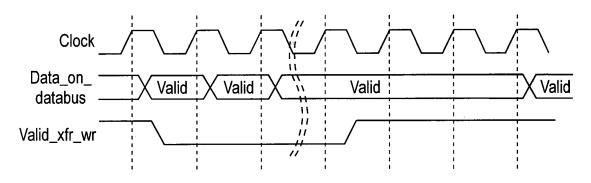


FIG. 22

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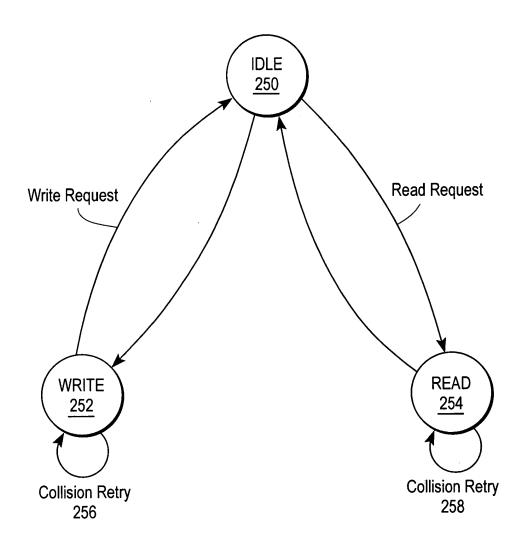


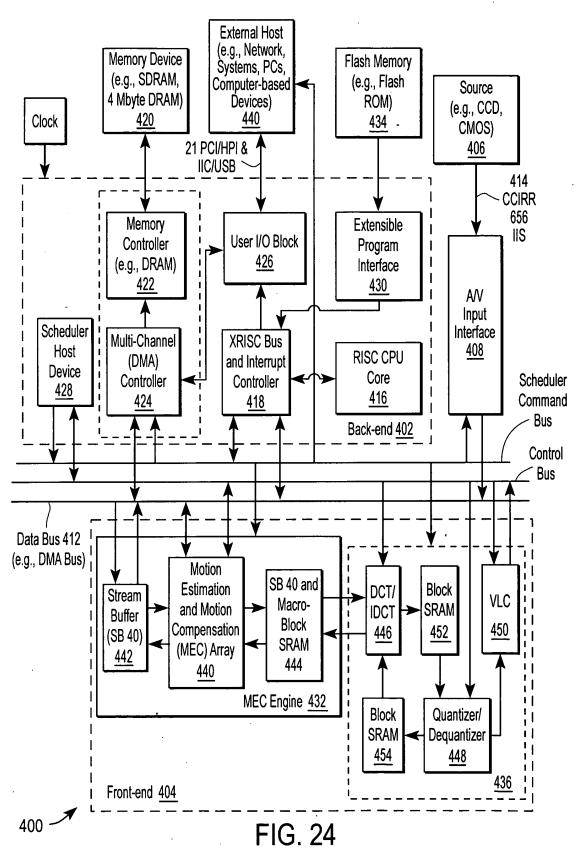
FIG. 23

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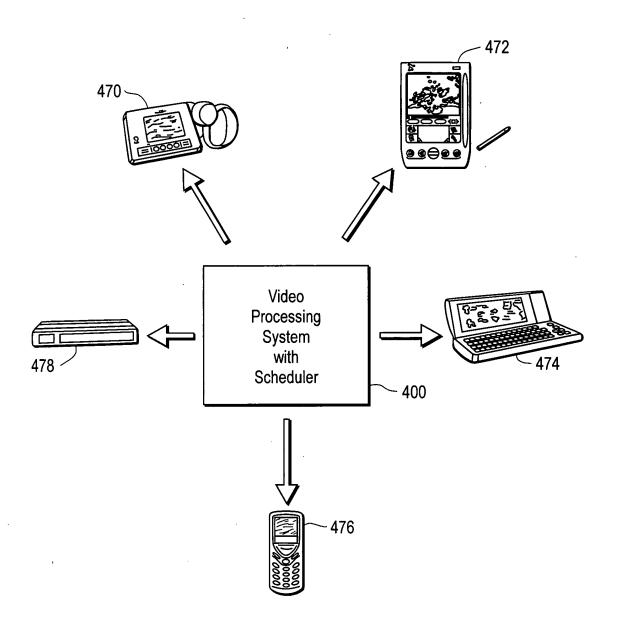


FIG. 25

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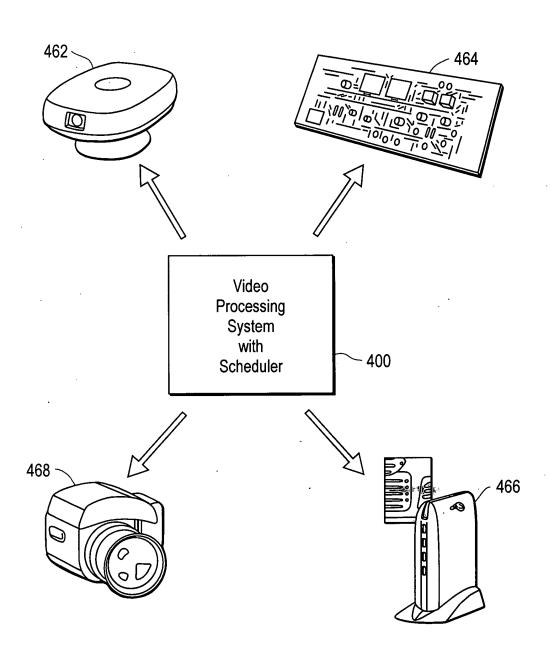


FIG. 26